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10/580,969	02/26/2007	Tony Albrecht	5367-237PUS	2543

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EXAMINER	
WARD, ERIC A	

ART UNIT	PAPER NUMBER
2891	

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02/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,969	ALBRECHT ET AL.	
	Examiner	Art Unit	
	ERIC WARD	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3,5-8,11-15,17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (U.S. Patent No. 6,185,240) (henceforth Jiang) in view of Sawai et al. (JP 57093591 Abstract) (henceforth Sawai).

Regarding **Claim 1**, Jiang discloses a light emitting semiconductor component (title) comprising a monolithically produced sequence of semiconductor layers (Fig. 1 items 109,111,119) (Col. 2 Lines 25-28), which comprise:

- An area of n-doped semiconductor layers (Fig. 1 item 109);
- An area of p-doped semiconductor layers (Fig. 1 item 119) following the area of n-doped semiconductor layers;

- A first pn junction formed between the n-doped area and the p-doped area (Fig. 1 item 111, specifically 115) (Col. 2 Lines 26-27);
- An insulating section (Fig. 1 item 133) dividing the first pn junction into a light-emitting section (i.e. immediately to the left of the insulating section) (see response to arguments) and a protective-diode section (i.e. right of the insulating section), wherein the insulating section electrically insulates the light-emitting section and the protective-diode section from one another in the area of the p-doped semiconductor layers, and
- Wherein the first pn junction has a larger area (Fig. 2 item 105) (Fig. 1 trench 133 has a width from between 0.1 to 100 microns) in the protective-diode section than in the light-emitting section (Fig. 2 item 122) (Fig. 1 trench 131 has a width from between 0.1 to 100 microns, *thereby inclusive of instances wherein the protective-diode section has a larger area*).

Jiang fails to expressly teach an n doped semiconductor portion provided in the protective-diode section and on a side of the area of p-doped semiconductor layers facing away from the first pn junction wherein the n-doped semiconductor portion forms a second pn junction with a first portion of the area of p-doped semiconductor layers in the protective-diode section and is electrically conductively connected to a second portion of the area of p-doped semiconductor layers in the light-emitting section. More generally, Jiang fails to expressly teach an N-P-N protective diode but rather a single protective N-P diode (see Fig. 3 attached below).

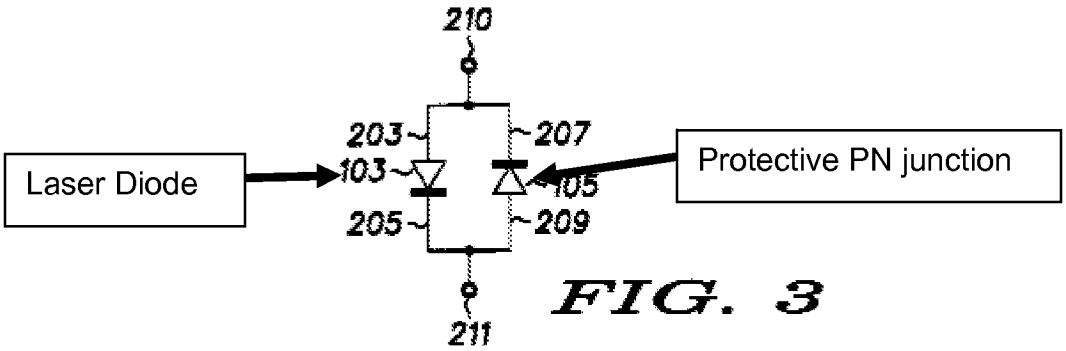
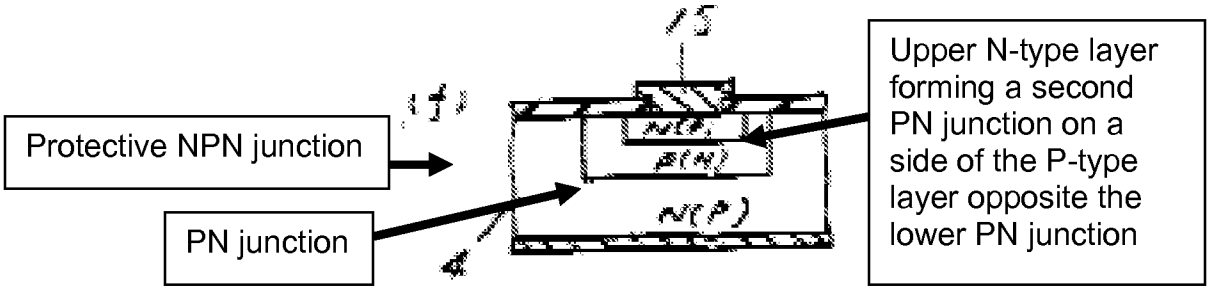
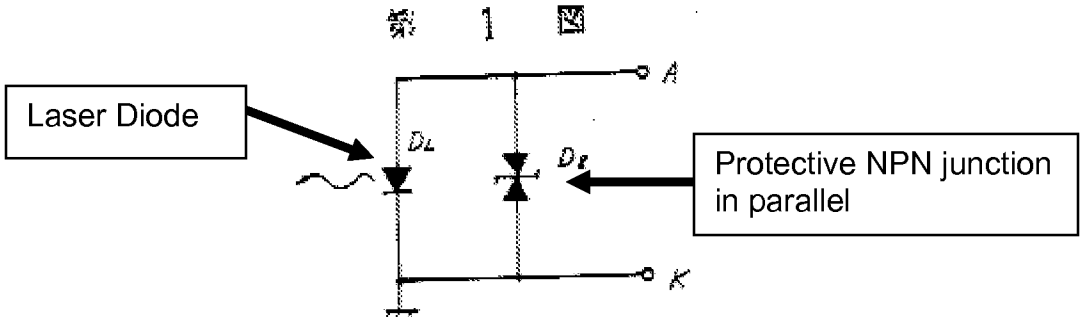


FIG. 3

Sawai teaches forming a laser diode chip having a first P-N junction and a protective diode having an N-P-N junction (see attached Fig. 4f below) in parallel (see attached Fig. 1) in order to regulate the surge rate during breakdown (abstract).





It would have been obvious at the time of the invention to one having ordinary skill in the art to have replaced the NP diode of Jiang with the NPN diode of Sawai such

that an n doped semiconductor portion provided in the protective-diode section and on a side of the area of p-doped semiconductor layers facing away from the first pn junction wherein the n-doped semiconductor portion forms a second pn junction with a first portion of the area of p-doped semiconductor layers in the protective-diode section and is electrically conductively connected to a second portion of the area of p-doped semiconductor layers in the light-emitting section, since the addition of a second pn junction in parallel with the first pn junction serves to regulate the surge rate during breakdown (Sawai Abstract).

Furthermore, Claim 1 does not expressly require that the n-doped semiconductor portion be **directly** electrically connected to a second portion of the area of p-doped semiconductor layers in the light emitting section and Fig. 1 of Sawai discloses the light emitting device 3 is connected to the protection diodes Dz in parallel (i.e. the same connection as the claimed invention), therefore the n-type layer (top layer, Fig. 4 item 13) of Sawai is electrically connected to the second portion of the area of p-doped semiconductor layers in the light emitting section by the wiring 5.

Regarding **Claim 2**, Jiang further discloses wherein the first pn junction has a larger area in the protective-diode section than in the light-emitting section by at least a factor of 100 (Col. 2 Lines 59-67, trench defining VCSEL ranges from 0.1 to 100 microns and trench defining diode ranges from 0.1 to 100 microns, thereby covering the range wherein the protective diode section has an area greater than at least a factor of 100).

Furthermore, it has been held in case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976) and similarly a prima facie case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. *Titanium Metals Corp. of America v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (See MPEP 2144.05 *Obviousness of Ranges I. OVERLAP OF RANGES*).

Furthermore, it has been held that where "the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) wherein in the instant case the area of the protective diode section and therefore the diode characteristics are a results effective variable since the area determines the discharge rate of electro-static charge and determining the general or optimum area by routine experimentation is within the capabilities of one having ordinary skill in the art (see MPEP 2144.05 *Obviousness of Ranges II. OPTIMIZATION OF RANGES A. Optimization Within Prior Art Conditions or Through Routine Experimentation* and *B. Only Result-Effective Variables Can Be Optimized*).

Regarding **Claim 3**, Jiang further discloses wherein the sequence of semiconductor layers is applied to a semiconductor substrate (Fig. 1 item 101) (Col. 1 Lines 66-67).

Regarding **Claim 5**, Jiang further discloses wherein the area of n-doped semiconductor layers (Fig. 1 item 109) is only partially interrupted by the insulating section (Fig. 1 item 133).

Regarding **Claim 6**, Jiang further discloses wherein the insulating section (Fig. 1 item 133) extends from a surface of the sequence of semiconductor layers opposite to the semiconductor substrate into the area of n-doped semiconductor layers (Fig. 1 item 109).

Regarding **Claim 7**, Jiang further discloses wherein the light-emitting section is formed by a vertical cavity surface emitting laser (VCSEL) (Col. 1 Lines 57-60).

Regarding **Claim 8**, Jiang further discloses wherein the first pn junction (Fig. 1 item 111) is arranged between a first sequence of Bragg reflector layers (Fig. 1 item 109) and a second sequence of Bragg reflector layers (Fig. 1 item 119), and wherein each of the first and second sequences has a multiplicity of layer pairs (as pictured), and the two sequences of Bragg reflector layers form a laser resonator (VCSEL, Col. 1 Lines 57-60), one of the two sequences of the Bragg reflector layers (Fig. 1 item 119) being semitransparent for a laser radiation generated in the first pn junction (in order to output light through Fig. 1 item 122) (Col. 2 Lines 38-41).

Regarding **Claim 11**, Jiang further discloses wherein the insulating section (Fig. 1 item 133) is constructed as a trench (Col. 2 Lines 31).

Regarding **Claim 12**, Jiang further discloses wherein the light-emitting section and the protective-diode section have a mesa-shaped structure (formed through lithography and etching) on a side of the trench.

Regarding **Claim 13**, Jiang further discloses wherein the trench (Fig. 1 item 133) is bounded by areas which are provided with an insulating layer Fig. 1 item 121) (Col. 2 Line 8).

Regarding **Claim 14**, Jiang further discloses wherein the trench (Fig. 1 item 133) is filled with a material from which the second contact metallization (Fig. 2 items 123,125) is formed.

Regarding **Claim 17**, Jiang discloses a light-emitting semiconductor component (title) comprising a monolithically produced sequence of semiconductor layers (Fig. 1 items 109,111,119) (Col. 2 Lines 25-28), which comprise:

- an area of n-doped semiconductor layers (Fig. 1 item 109);
- an area of p-doped semiconductor layers (Fig. 1 item 119) following the area of n-doped semiconductor layers;

- a first pn junction formed between the areas (Fig. 1 item 111, specifically 115) (Col. 2 Lines 26-27);
- an insulating section (Fig. 1 item 133) dividing the first pn junction into a light-emitting section (i.e. immediately to the left of the insulating section) (see response to arguments) and a protective-diode section (i.e. right of the insulating section) wherein the insulating section electrically insulates the light-emitting section and the protective-diode section from one another in the area of p-doped semiconductor layers,
- wherein the first pn junction in the area of the protective-diode section is short circuited (Fig. 1 item 169 short circuits the first pn junction)

Jiang fails to expressly teach an n-doped semiconductor provided in the protective-diode section on a side of the area of p-doped semiconductor layers facing away from the first pn junction wherein the n-doped semiconductor portion forms a second pn junction with a first portion of the area of p-doped semiconductor layers in the protective-diode section and is electrically conductively connected to a second portion of the area of p-doped semiconductor layers in the light-emitting section.

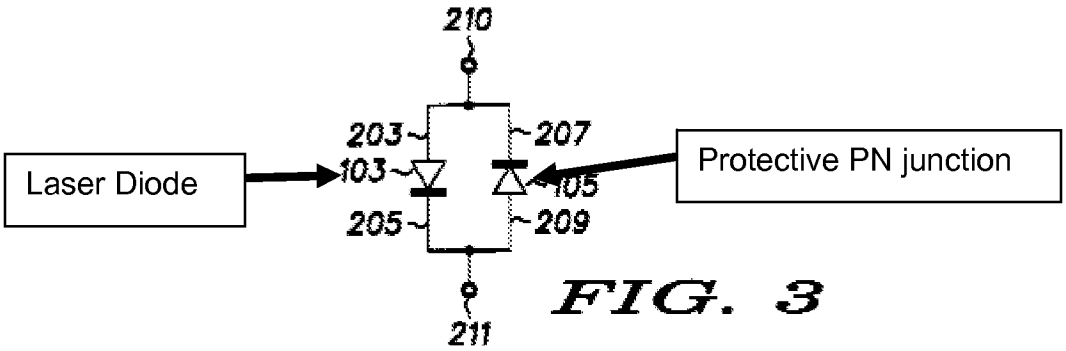
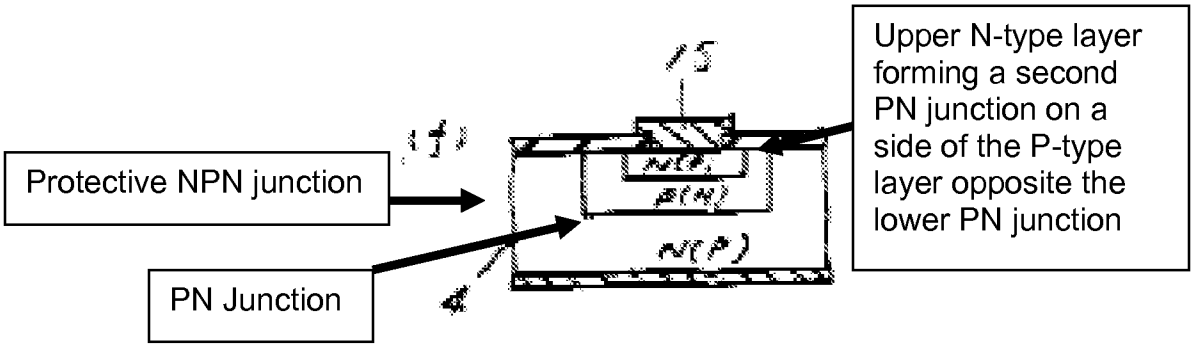
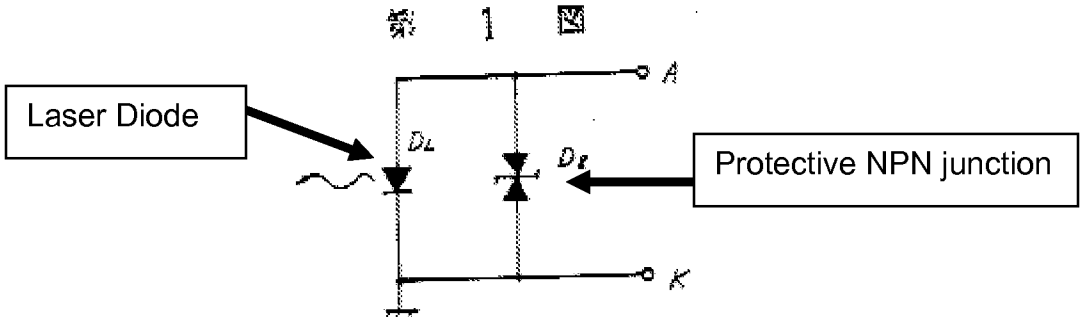


FIG. 3

Sawai teaches forming a laser diode chip having a first P-N junction and a protective diode having an N-P-N junction (see attached Fig. 4f below) in parallel (see attached Fig. 1) in order to regulate the surge rate during breakdown (abstract).





It would have been obvious at the time of the invention to one having ordinary skill in the art to have replaced the NP diode of Jiang with the NPN diode of Sawai such

that an n doped semiconductor portion is provided in the protective-diode section and on a side of the area of p-doped semiconductor layers facing away from the first pn junction wherein the n-doped semiconductor portion forms a second pn junction with a first portion of the area of p-doped semiconductor layers in the protective-diode section and is electrically conductively connected to a second portion of the area of p-doped semiconductor layers in the light-emitting section, since the addition of a second pn junction in parallel with the first pn junction serves to regulate the surge rate during breakdown (Sawai Abstract).

Furthermore, Claim 17 does not expressly require that the n-doped semiconductor portion be **directly** electrically connected to a second portion of the area of p-doped semiconductor layers in the light emitting section and Fig. 1 of Sawai discloses the light emitting device 3 is connected to the protection diodes Dz in parallel (i.e. the same connection as the claimed invention), therefore the n-type layer (top layer, Fig. 4 item 13) of Sawai is electrically connected to the second portion of the area of p-doped semiconductor layers in the light emitting section by the wiring 5.

Regarding **Claim 18**, Jiang further discloses wherein an electrically conductive layer (Fig. 1 item 169) is applied to a side edge (inside right edge of Fig. 1 trench 137) of the sequence of semiconductor layers facing the protective-diode section and electrically connects the area of n-doped semiconductor layers and the area of p-doped semiconductor layers with one another.

Regarding **Claim 19**, Jiang discloses a light-emitting semiconductor component (title) comprising a monolithically produced sequence of semiconductor layers (Fig. 1 items 109,111,119) (Col. 2 Lines 25-28), which comprise:

- an area of p-doped semiconductor layers (Fig. 1 item 109);
- an area of n-doped semiconductor layers (Fig. 1 item 119) following the area of p-doped semiconductor layers;
- a first pn junction (Fig. 1 item 111, specifically item 115) formed between the p-doped area and the n-doped area;
- an insulating section (Fig. 1 item 133) dividing the first pn junction into a light-emitting section (i.e. immediately to the left of the insulating section) (see response to arguments) and a protective-diode section (i.e. right of the insulating section), wherein the insulating section electrically insulates the light-emitting section and the protective-diode section from one another in the area of n-doped semiconductor layers, and
- wherein the first pn junction has a larger area (Fig. 2 item 105) (Fig. 1 trench 133 has a width from between 0.1 to 100 microns) in the protective-diode section than in the light-emitting section (Fig. 2 item 122) (Fig. 1 trench 131 has a width from between 0.1 to 100 microns, *thereby inclusive of instances wherein the protective-diode section has a larger area).*

Jiang fails to expressly teach a p-doped semiconductor portion provided in the protective-diode section and on a side of the area of n-doped semiconductor layers

facing away from the first pn junction, wherein the p-doped semiconductor portion forms a second pn junction with a first portion of the area of n-doped semiconductor layers in the protective-diode section and is electrically conductively connected to a second portion of the area of n-doped semiconductor layers in the light-emitting section. More generally, Jiang fails to expressly teach a P-N-P protective diode but rather a single protective N-P diode.

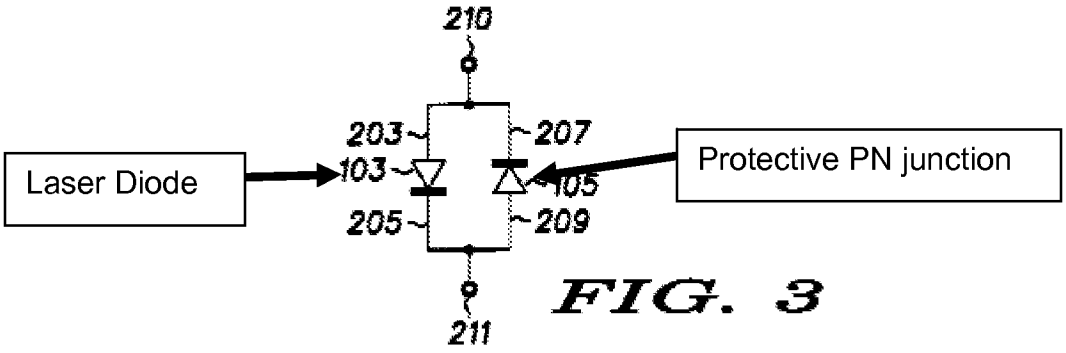
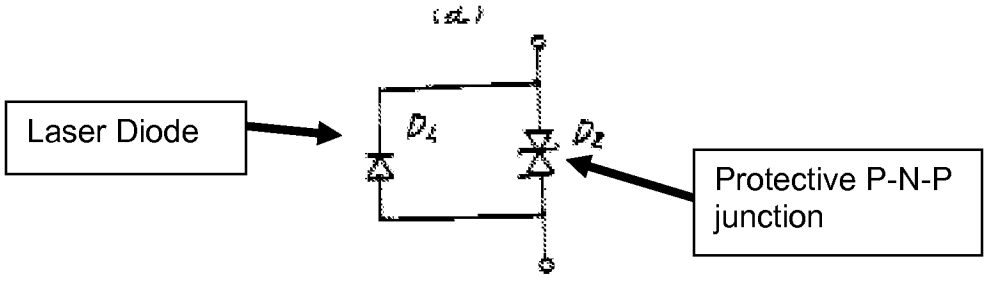


FIG. 3

Sawai teaches forming a laser diode chip having a first P-N junction and a protective diode having an P-N-P junction (see attached Fig. 6d below) in parallel in order to regulate the surge rate during breakdown (abstract).



It would have been obvious at the time of the invention to one having ordinary skill in the art to have replaced the NP diode of Jiang with the PNP diode of Sawai such that an n doped semiconductor portion is provided in the protective-diode section and on a side of the area of p-doped semiconductor layers facing away from the first pn junction wherein the n-doped semiconductor portion forms a second pn junction with a first portion of the area of p-doped semiconductor layers in the protective-diode section and is electrically conductively connected to a second portion of the area of p-doped semiconductor layers in the light-emitting section, since the addition of a second pn junction in parallel with the first pn junction serves to regulate the surge rate during breakdown (Sawai Abstract).

Furthermore, Claim 19 does not expressly require that the p-doped semiconductor portion be **directly** electrically connected to a second portion of the area of n-doped semiconductor layers in the light emitting section and Fig. 1 of Sawai discloses the light emitting device 3 is connected to the protection diodes Dz in parallel (i.e. the same connection as the claimed invention), therefore the p-type layer (top layer, Fig. 4 item 13) of Sawai is electrically connected to the second portion of the area of n-doped semiconductor layers in the light emitting section by the wiring 5.

Claim 4,9 and 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 6,185,240) (henceforth Jiang) in view of Sawai et al. (JP 57093591 Abstract) (henceforth Sawai) as applied to Claims above, further in view of Dowd et al (US 6,639,931) (henceforth Dowd).

Regarding **Claim 4**, Jiang further discloses a first contact metallization (Fig. 1 item 123) applied to a side of the semiconductor substrate and a second contact metallization (Fig. 1 item 125) (Col. 3 Lines 46-49) applied to a surface of the sequence of semiconductor layers on to the semiconductor substrate.

Jiang fails to expressly teach wherein the first contact metallization is applied to a side of the semiconductor substrate facing away from the sequence of semiconductor layer (i.e. Jiang teaches a lateral contact structure rather than a back lower contact) (Col. 3 Line 65 to Col. 4 Line 6).

Dowd teaches forming a back lower contact (Fig. 2 item 8) (Col. 1 Line 15).

It would have been obvious at the time of the invention to one having ordinary skill in the art to have formed the device of Jiang with a back contact as taught by Dowd in order to make use of the back-side of the substrate leading to a more compact device.

Regarding **Claim 9**, Jiang fails to expressly teach wherein in one of the two sequences of Bragg reflector layers, at least one current aperture is provided for spatially limiting an operating current flowing through the first pn junction in the light-emitting section during

the operation of the vertical cavity surface emitting laser. Jiang omits some engineering details (Col. 2 Lines 15-18).

Dowd teaches wherein a typical VCSEL, one of the two sequences of Bragg reflector layers (Fig. 2 items 4 and 5) (Col. 1 Lines 7-21) includes a current aperture (Fig. 2 item 9) is provided for spatially limiting an operating current flowing through the first pn junction in a light-emitting section during the operation of a vertical cavity surface emitting laser.

It would have been obvious at the time of the invention to one having ordinary skill in the art to have included a current aperature as taught by Dowd in order to create a functional and operating VCSEL (Dowd Col. 1 Lines 10-12).

Regarding **Claim 10**, Jiang further discloses wherein the second contact metallization (Fig. 2 item 123) partially covers a surface of the light-emitting section (Fig. 1 and Fig. 2 item 122) in such a manner that an uncovered area of the light-emitting section remains as light exit opening.

Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US 6,185,240) (henceforth Jiang `240) in view of Sawai et al. (JP 57093591 Abstract) (henceforth Sawai), further in view of Jiang et al. (US 5,757,836) (henceforth Jiang `836).

Jiang `240 fails to expressly teach wherein the insulating section is formed by an implantation, diffusion or oxidation process.

Jiang `836 teaches a VCSEL having an insulating section (Fig. 2 and 3 items 51 and 52) (Col. 3 Lines 57-67) forming insulating sections by an implantation process.

It would have been obvious at the time of the invention to one having ordinary skill in the art to have modified the device of Jiang `240 with the implant isolation regions as taught by Jiang `836 in order to effectively insulate VCSELs from adjacent components as well as absorb spontaneous lateral emission (Jiang `836 Col. 4 Lines 4-9).

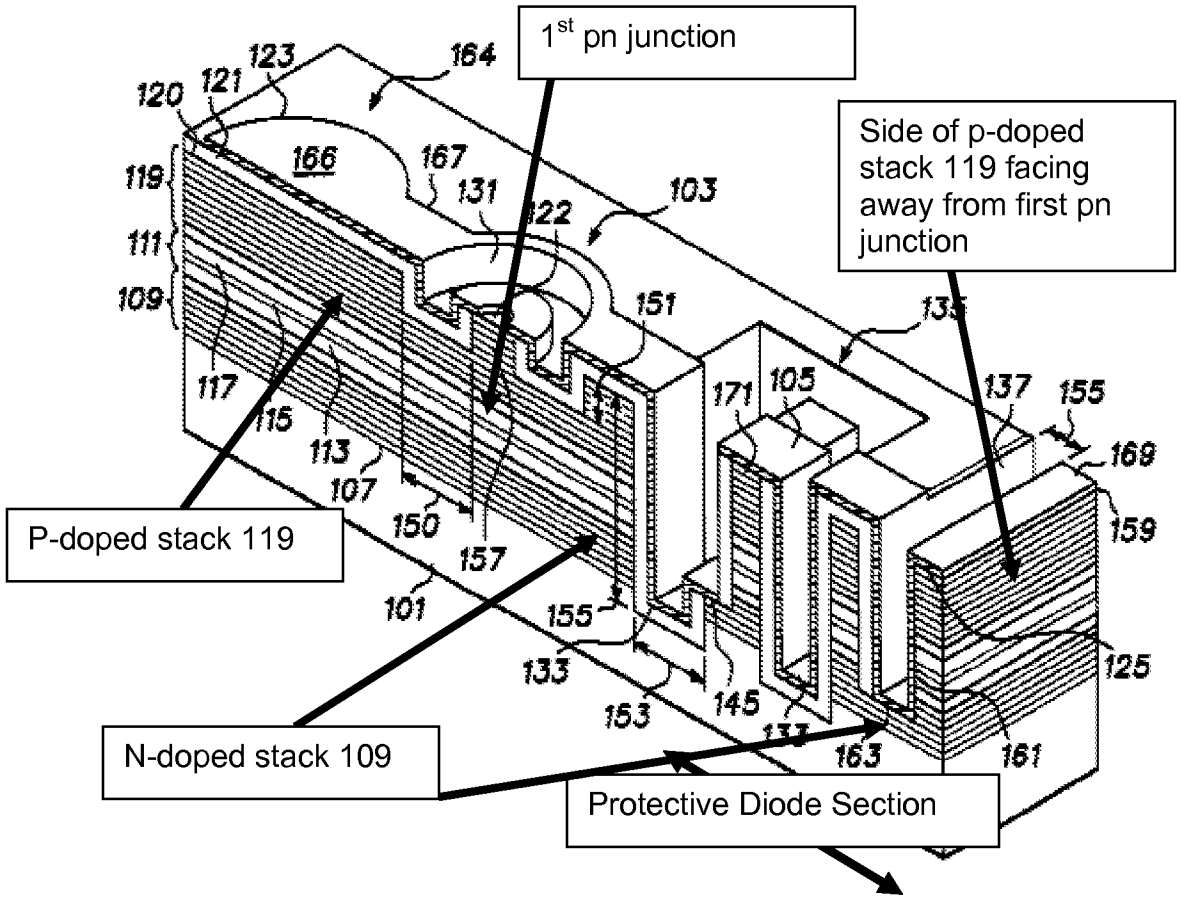
Response to Arguments

Applicant's arguments filed 11/10/2008 have been fully considered but they are **only partially persuasive**.

Applicants argue that:

> (i) the stack 109 in Jiang is not "provided in the protective-diode section and on a side of the area of p-doped semiconductor layers facing away from the first pn junction," as is the "n-doped semiconductor layer" recited in independent claim 1;

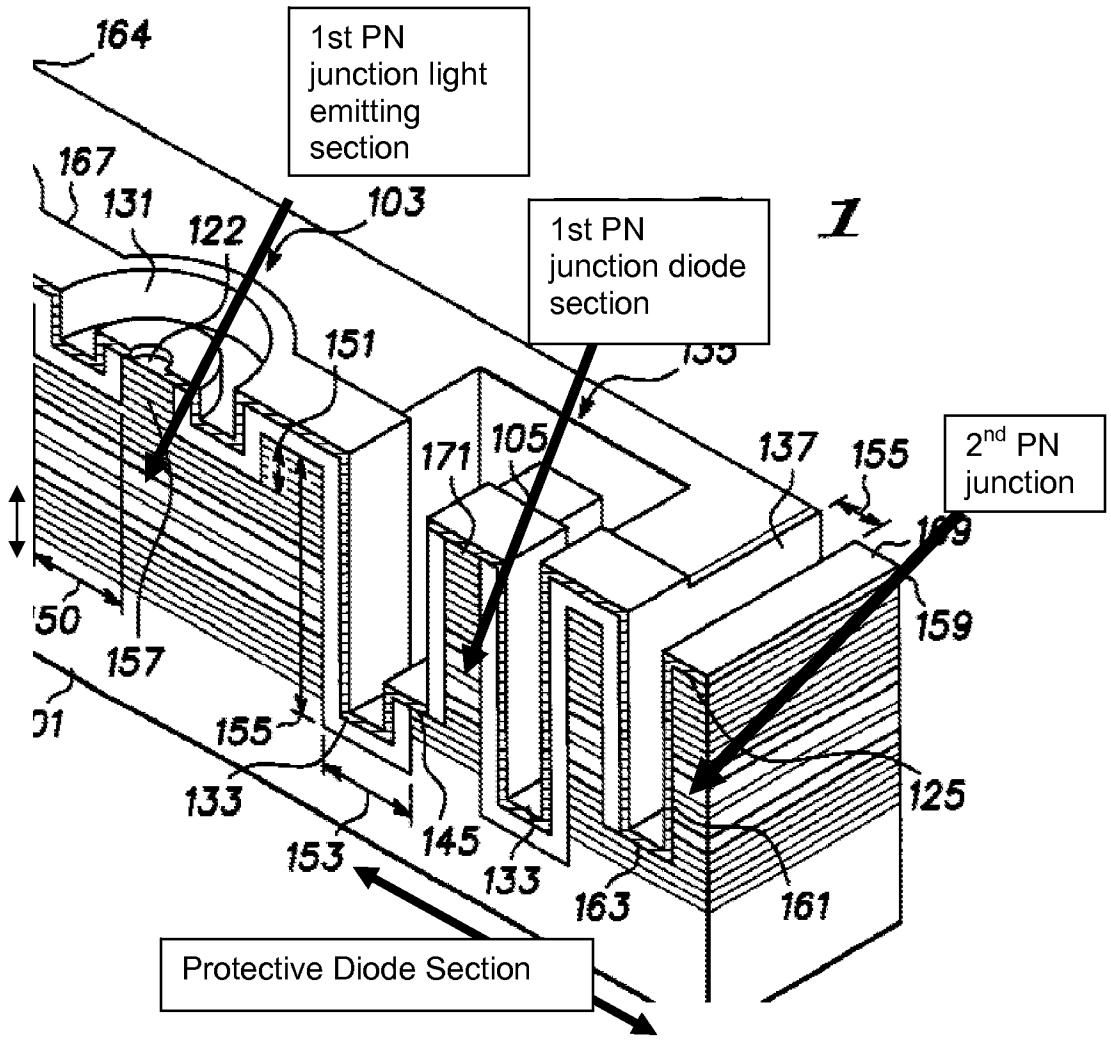
However, this is **not persuasive** as stack 109 is provided on a side of the area of p-doped semiconductor layers facing away from the first pn junction as shown below.



Applicants further argue that

(ii) the alleged second pn junction in Jiang is not formed "in the protective-diode section," as recited in independent claim 1;

However, this is **not persuasive** since the second pn junction of Jiang is indeed formed in the protective diode region as is shown below.



Applicants further argue

(iii) neither one of the conductive layers 123, 125 in Jiang is "the n-doped semiconductor portion ... electrically conductively connected to a second portion of the area of p-doped semiconductor layers in the light-emitting section," as recited in independent claim 1;

This **is persuasive**, as the region of n-type conductive layers identified as the second PN junction (see above) in Jiang does is not directly electrically connected to the p-doped semiconductor layers in the light-emitting section (i.e. does not form an PNP junction).

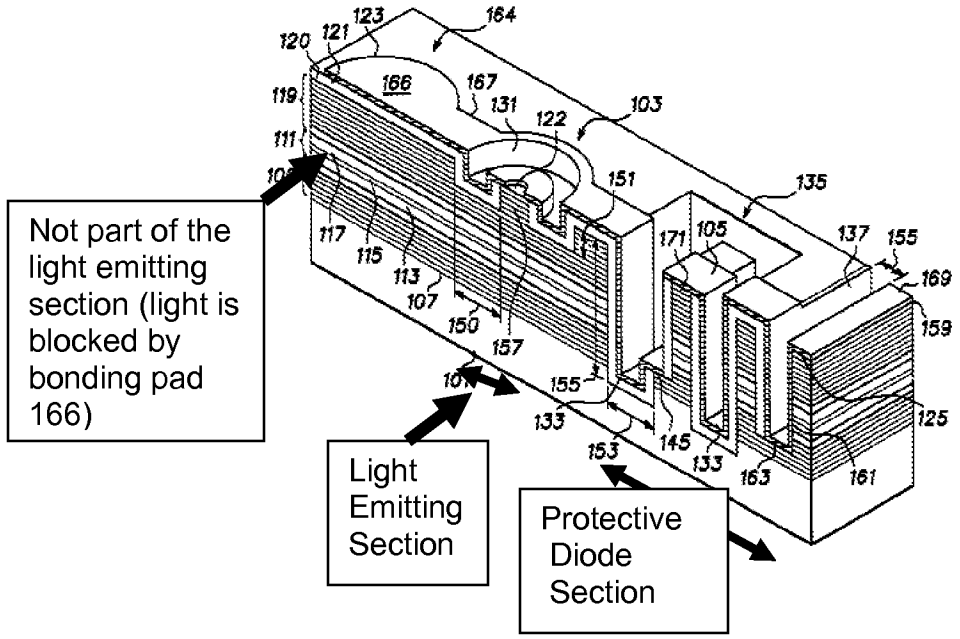
Applicants further argue

(iv) the diode 105 and the orifice 122 in Jiang are not part of the first pn junction; therefore the comparison of Jiang's diode 105 and orifice 122 made in the Office Action is irrelevant to the claim features that "the first pn junction has a larger area in the protective-diode section than in the light-emitting section," as recited in independent claim 1.

This is **not persuasive** as Applicants appear to identify the light emitting section as the entire region to the left on the insulating trench 133, wherein *one having ordinary skill in the art would reasonably interpret* ***only*** *the region* ***acting*** *as a light emitting region as the light emitting region* (see attached below).

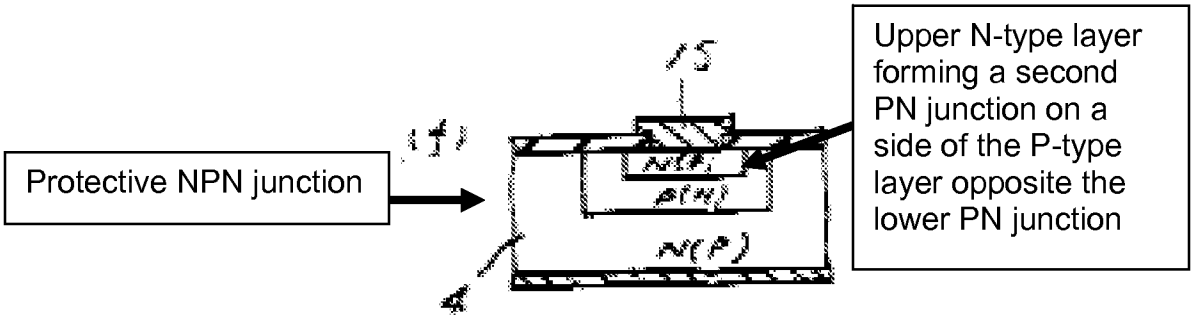
Furthermore, Jiang discloses in Col. 4 wherein dimensions may be adjusted for high electrostatic breakdown

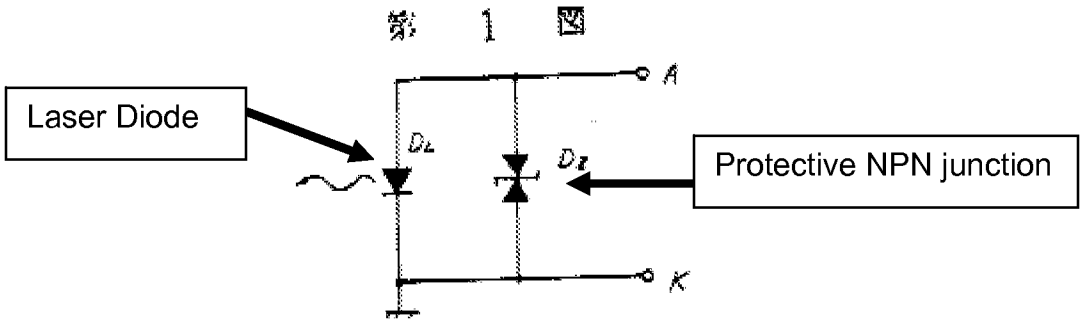
It will be understood that diode **105** can be fabricated in a variety of embodiments but in the preferred embodiment diode **105** is a p-i-n diode. Further, depending upon materials, etc. the breakdown voltage of diode **105** can be a relatively wide range but should be at least sufficient to withstand and discharge any expected ESD events. Generally the range of breakdown voltages can be from 10s to several hundred volts. VCSEL **103** and diode **105** are electrically coupled at contacts **210** and **211**. By electrically coupling VCSEL **103** with diode **105**, the reverse biased ESD damage threshold of VCSEL **103** is increased to at least the level of the forward biased ESD damage threshold, which is typically at least 100–200 Volts higher. Thus, the reliability of VCSEL **103** is improved due to the decreasing likelihood of catastrophic failure of VCSEL **103** by an ESD event.



Applicants further argue on Page 15 that Sawai does not teach "the first pn junction has a larger area in the protective-diode section and a light emitting section;" however, Sawai is not relied upon for teaching this feature.

Applicants further argue on Page 15 that Sawai does not teach “the n-doped semiconductor portion forms a second pn junction ... in the protective diode section and is electrically connected to a second portion of the area of p-doped semiconductor layers in the light emitting section." First, Sawai is not relied upon for teaching a protective diode section or light emitting section. Second, Sawai teaches forming the n-doped semiconductor in a second pn junction which is electrically connected to a section portion of the p-doped semiconductor layers of the laser diode as shown below.





Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC WARD whose telephone number is (571)270-3406. The examiner can normally be reached on M-T 5:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 5712721236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eric Ward/

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826